

## CLAIMS

- 1 1. A fail-safe system for differential current logic receiver circuits, wherein a fail-  
2 safe condition includes receiver inputs that are, floating, undriven, shorted together, or  
3 one or both shorted to ground, the fail-safe system comprising:  
4 a current mode differential receiver defining first and second inputs,  
5 a first driver of current into the first input and a second driver of current into the  
6 second input, wherein the first and the second currents are not equal to each other under  
7 normal operation,  
8 means for sensing the unequal currents and outputting a differential current corre-  
9 sponding to the received unequal currents, wherein in any defined fail-safe conditions the  
10 differential current output of the means for sensing remains stable.
- 1 2. The fail-safe system of claim 1 wherein the means for sensing comprises:  
2 means for establishing a differential current threshold wherein when the threshold  
3 is reached the means for sensing outputs a changed logic state.
- 1 3. The fail-safe system of claim 1 further comprising:  
2 a differential current amplifier arranged to accept the differential current output of  
3 the means for sensing and provide an amplified current, and  
4 a current to voltage converter that accepts the amplified current and outputs a  
5 voltage signal consistent with logic system.
- 1 4. The fail-safe system of claim 1 further comprising a resistor connected between  
2 the first and the second inputs.
- 1 5. The fail-safe system of claim 1 wherein the means for sensing comprises:  
2 a first current receiving circuit connected between the first input and a current re-  
3 turn path back to the current drivers,

4           a second current receiving circuit connected between the second input and a cur-  
5   rent return path back to the current drivers.

1   6.       The fail-safe system of claim 5 wherein the first and second current receiving cir-  
2   cuits comprise diode connected MOS transistors.

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1   7.       The fail-safe system of claims 6 further comprising means for biasing each diode  
2   connected MOS transistor so that each presents a given impedance to a current return  
3   path to the current drivers.

1   8.       The fail-safe system of claim 5 further comprising means for comparing the cur-  
2   rents in the first receiving circuit to the current in the second receiving circuit.

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1   9.       The fail-safe system of claim 8 wherein the means for comparing comprise:  
2           a first amplifying current mirroring circuit providing a first mirrored output cur-  
3   rent of the current received by the first receiving circuit,  
4           a second amplifying current mirroring circuit providing a second mirrored output  
5   current of the current received by the second receiving circuit, and  
6           a current to voltage conversion circuit, arranged to receive the first and the second  
7   output currents and provide a voltage output that is proportional to the difference between  
8   the outputs of the first and the second amplifying current mirroring circuits.

1   10.      A method for generating a fail-safe condition system for differential current logic  
2   receiver circuits when receiver inputs are: floating, undriven, shorted together, or one or  
3   both shorted to ground, the method comprising the steps of:

4           receiving external differential noise currents with a current mode differential re-  
5   ceiver defining first and second inputs,

6           driving a first current into the first input and a second current into the second in-  
7   put, wherein the difference between external current noise on differential data lines is

8 usually not big enough to overcome the threshold set by the failsafe bias transistors inter-  
9 nally under failsafe condition,  
10 sensing the unequal currents efficiently while under normal operation, and  
11 outputting a stable known state while under fail-safe conditions.

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